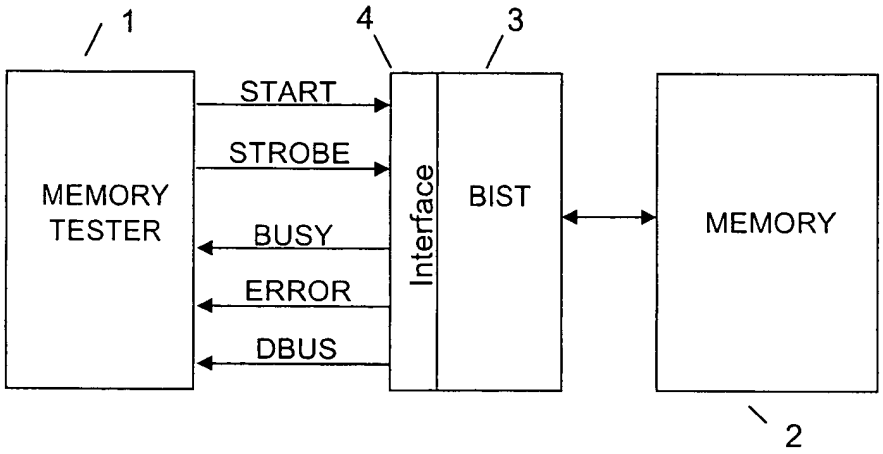
1
4
3
START
STROBE
BUSY
ERROR
DBUS
MEMORY TESTER
Interface
BIST
MEMORY
2

FIG. 1a

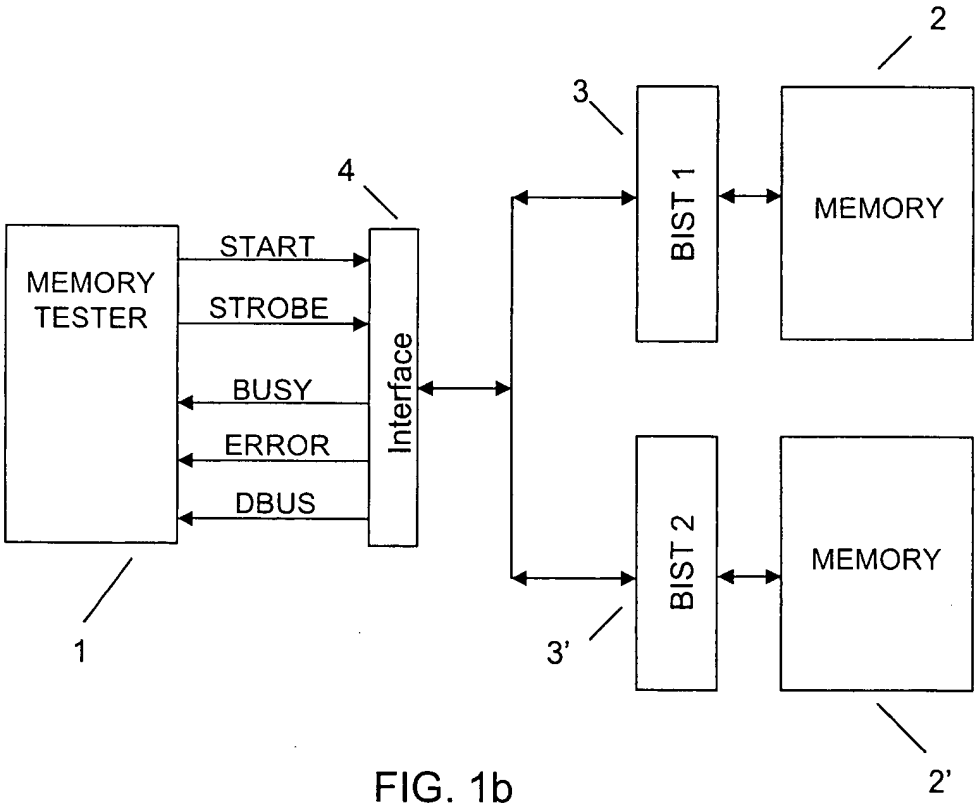
2
3
4
START
STROBE
BUSY
ERROR
DBUS
MEMORY TESTER
Interface
BIST 1
MEMORY
BIST 2
MEMORY
1
3'
2'

FIG. 1b

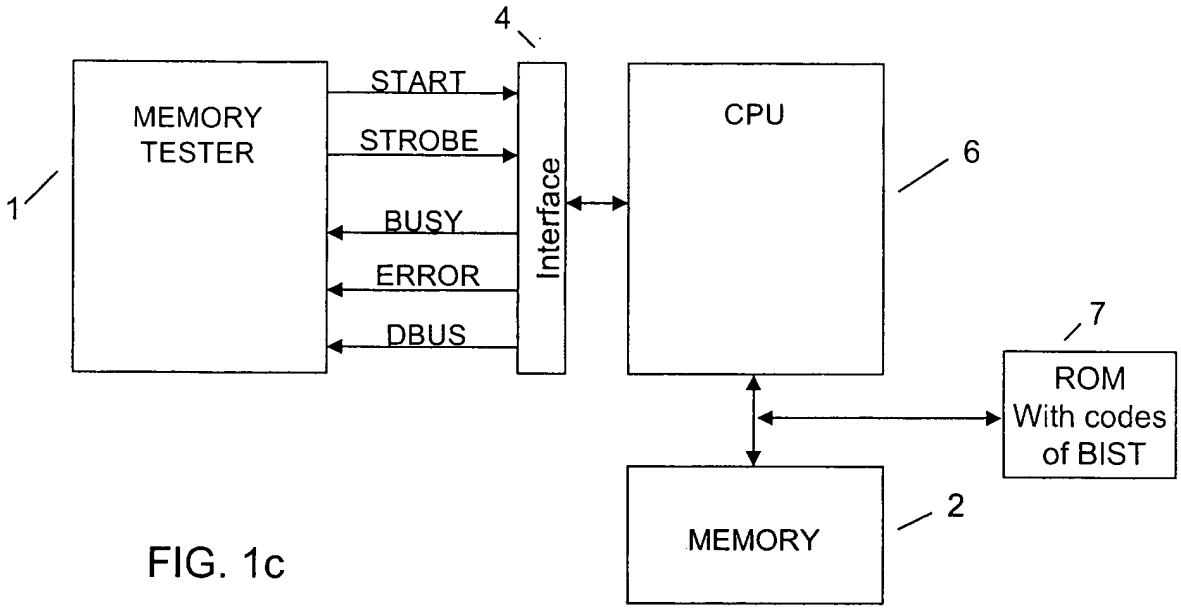
4
MEMORY TESTER
1
START
STROBE
BUSY
ERROR
DBUS
Interface
CPU
6
7
ROM With codes of BIST
MEMORY
2

FIG. 1c

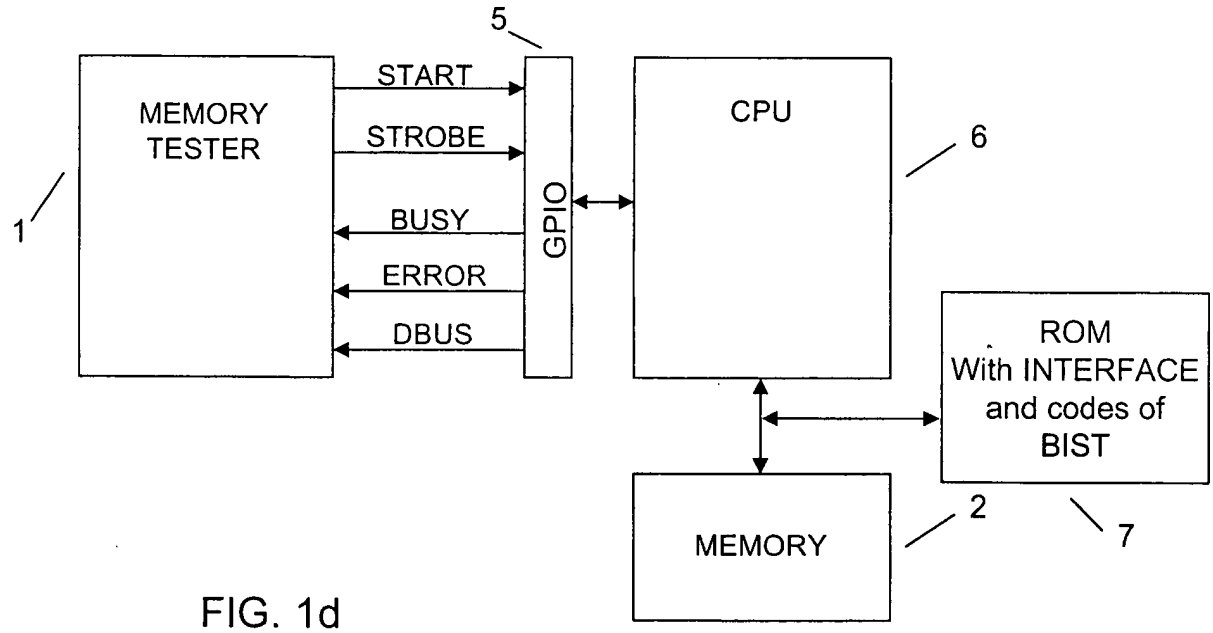
5
MEMORY TESTER
1
START
STROBE
BUSY
ERROR
DBUS
GPIO
CPU
6
ROM With INTERFACE and codes of BIST
7
MEMORY
2

FIG. 1d

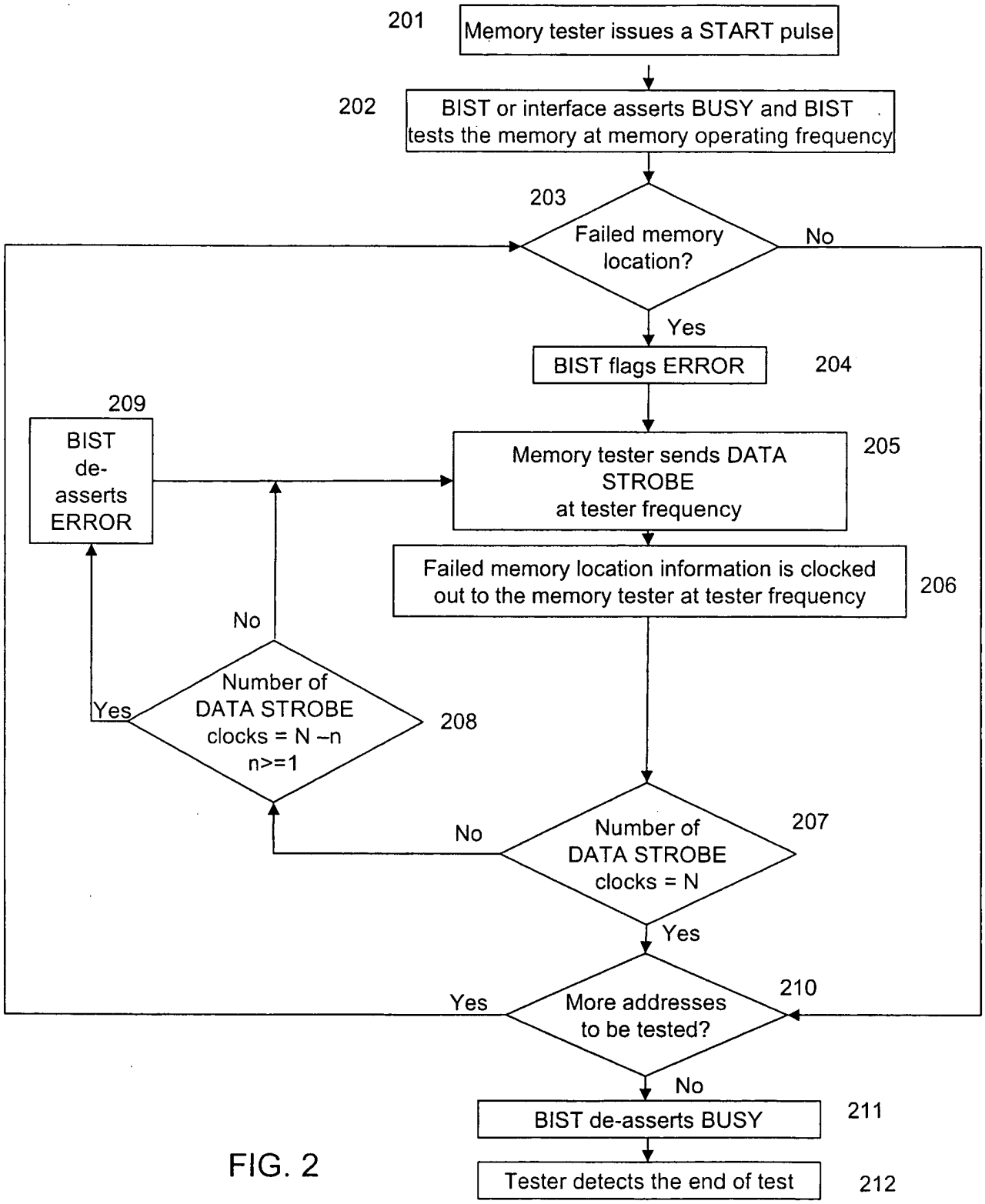
201
Memory tester issues a START pulse
202
BIST or interface asserts BUSY and BIST tests the memory at memory operating frequency
203
Failed memory location?
No
Yes
BIST flags ERROR
204
209
BIST de-asserts ERROR
Memory tester sends DATA STROBE at tester frequency
205
Failed memory location information is clocked out to the memory tester at tester frequency
206
No
Number of DATA STROBE clocks = N –n n>=1
Yes
208
No
Number of DATA STROBE clocks = N
207
Yes
Yes
More addresses to be tested?
210
No
BIST de-asserts BUSY
211
Tester detects the end of test
212

FIG. 2

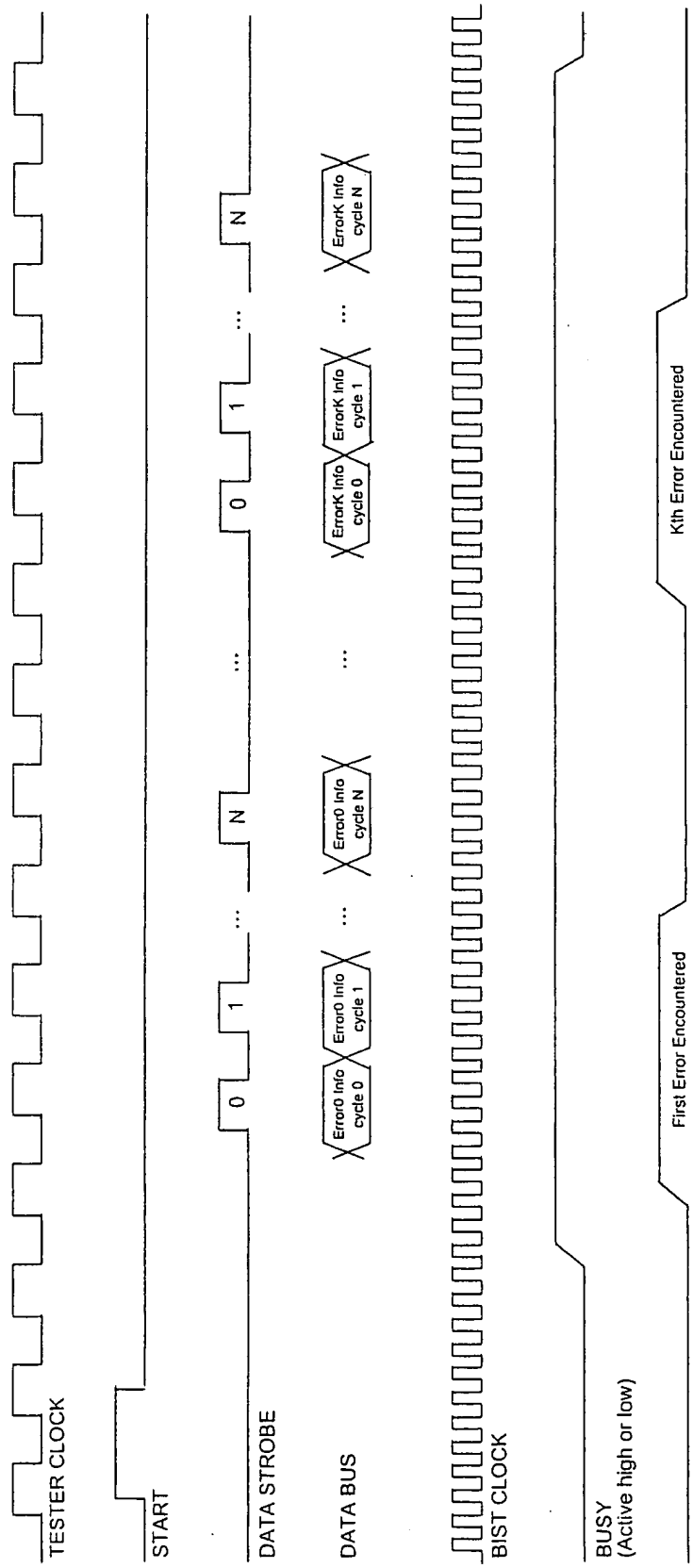
TESTER CLOCK
START
DATA STROBE
DATA BUS
BIST CLOCK
BUSY
(Active high or low)
ERROR
0
1
...
N
Error0 Info cycle 0
Error0 Info cycle 1
Error0 Info cycle N
ErrorK Info cycle 0
ErrorK Info cycle 1
ErrorK Info cycle N
First Error Encountered
Kth Error Encountered

Fig. 3

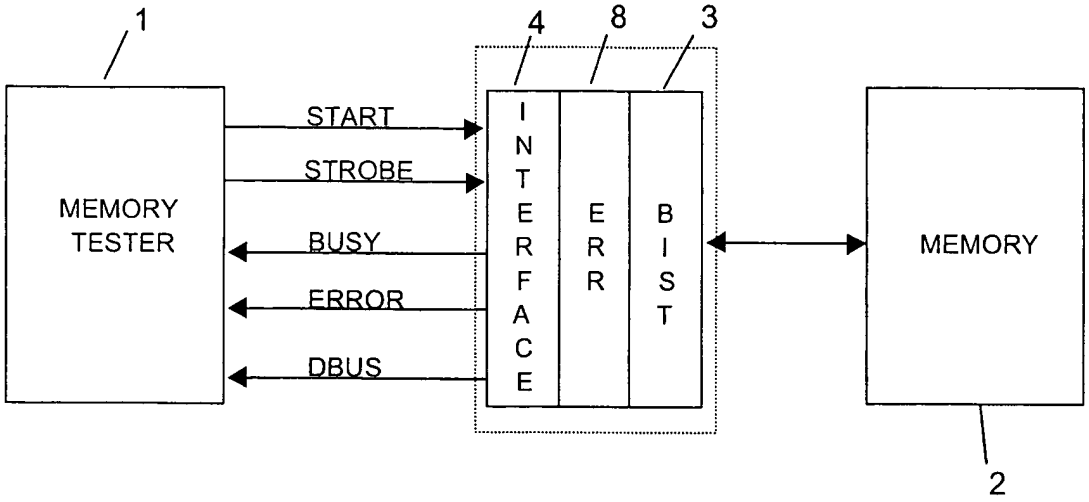
1
4
8
3
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
INTERFACE
ERR
BIST
MEMORY
2

FIG. 4a

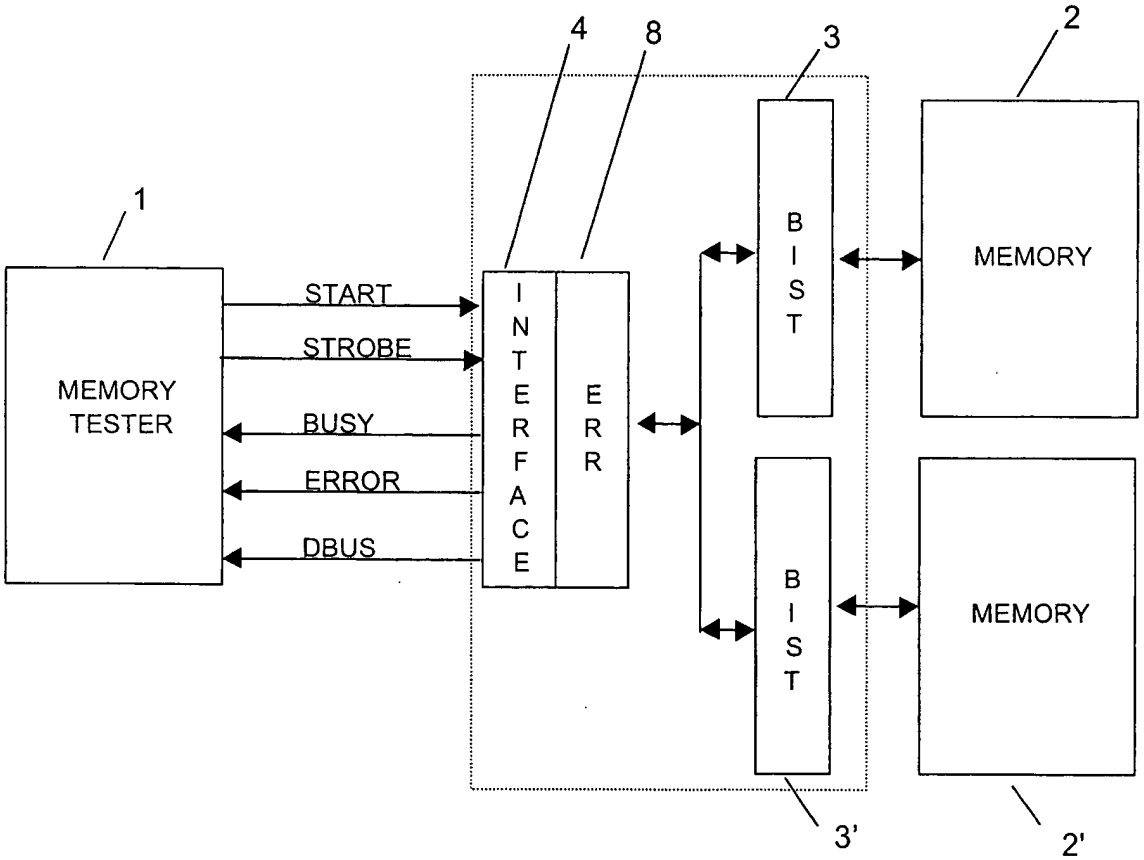
4
8
3
2
1
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
INTERFACE
ERR
BIST
MEMORY
BIST
MEMORY
3'
2'

FIG. 4b

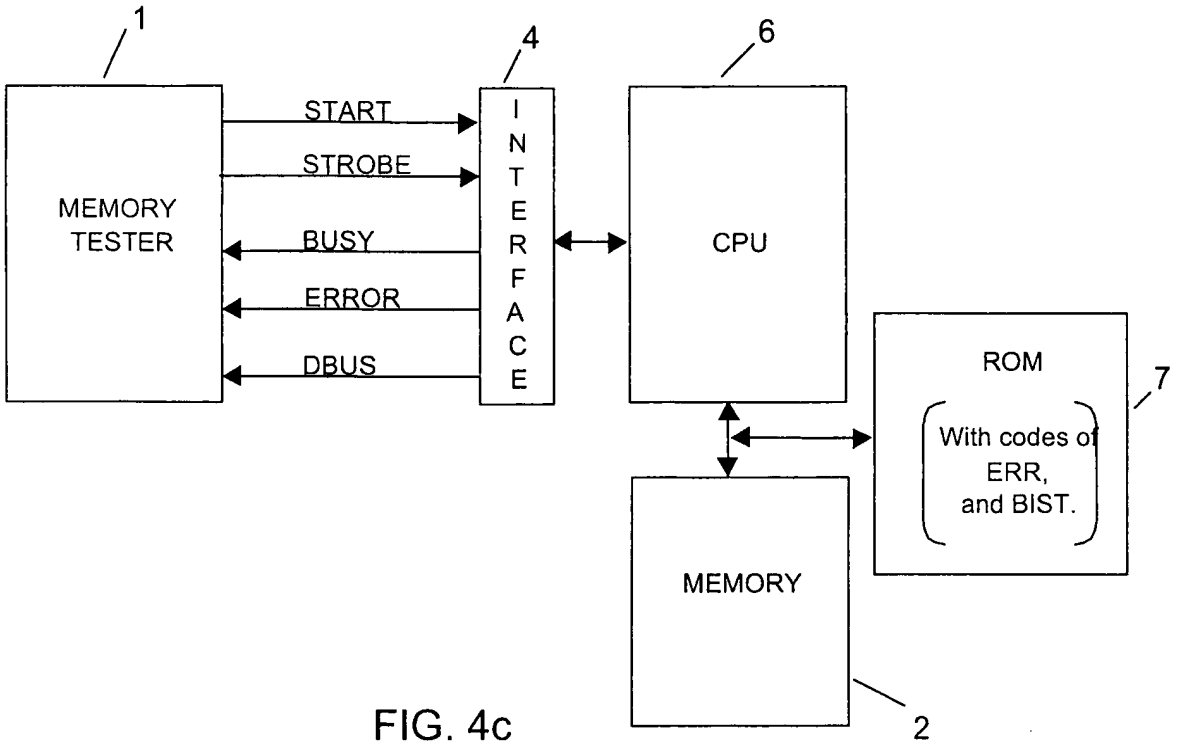
1
4
6
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
INTERFACE
CPU
ROM
With codes of ERR, and BIST.
7
MEMORY
2

FIG. 4c

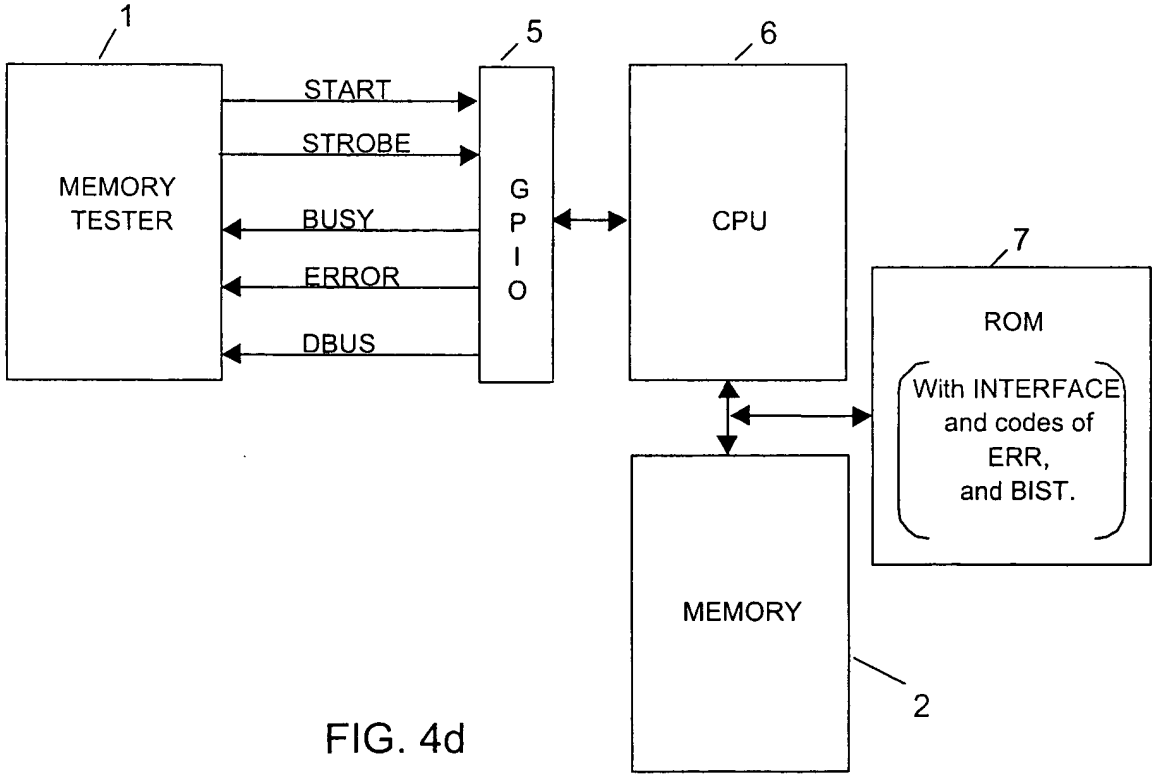
1
5
6
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
GPIO
CPU
7
ROM
With INTERFACE and codes of ERR, and BIST.
MEMORY
2

FIG. 4d

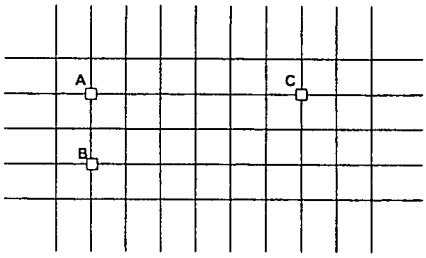

Fig. 5a

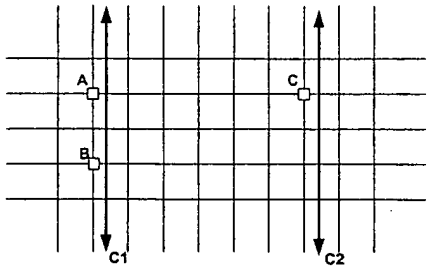

Fig. 5b

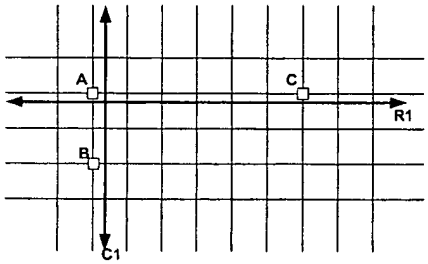

Fig. 5c

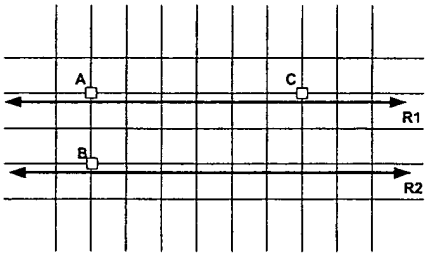

Fig. 5d

	ROW	COLUMN	BIT POSITION	EV	RGT1	RGTX	CGT1	CGTX	RF	CF
0	Row Addr A	Col Addr A	(A) I/O error Positions	1	1	0	1	0		
. . .										
N										

BAD LIST
(BL)

Fig. 5e

	ROW	COLUMN	BIT POSITION	EV2	RF2	CF2
←	Row Addr B	Col Addr C	(C) I/O error Positions	1		
←						
←						
←						

ASSOCIATED BAD LIST
(ABL)

Fig. 5f

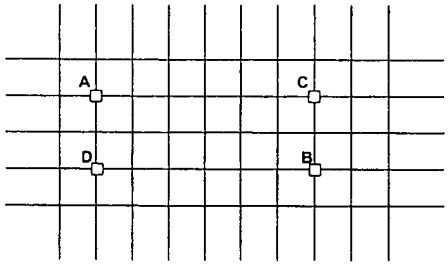

Fig. 6a

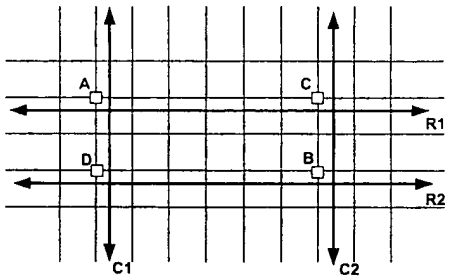

Fig. 6b

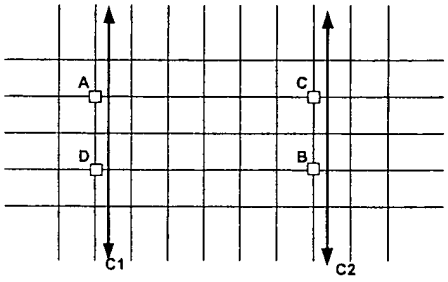

Fig. 6c

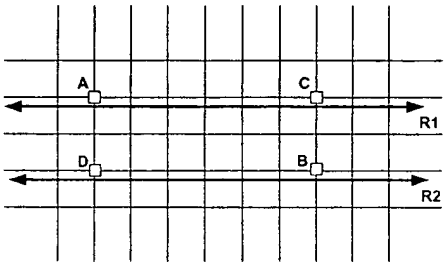

Fig. 6d

	ROW	COLUMN	BIT POSITION	EV	RGT1	RGTX	CGT1	CGTX	RF	CF
0	Row Addr A	Col Addr A	(A) I/O error Positions	1	1	0	1	0		
.	Row Addr B	Col Addr B	(B) I/O error Positions	1	1	0	1	0		
.				0						
N				0						

BAD LIST (BL)

Fig. 6e

	ROW	COLUMN	BIT POSITION	EV2	RF2	CF2
←	Row Addr D	Col Addr C	(C) I/O error Positions	1		
←	Row Addr C	Col Addr D	(D) I/O error Positions	1		
←				0		
←				0		

ASSOCIATED BAD LIST (ABL)

Row Addr B = Row Addr D
Col Addr B = Col Addr C

Fig. 6f

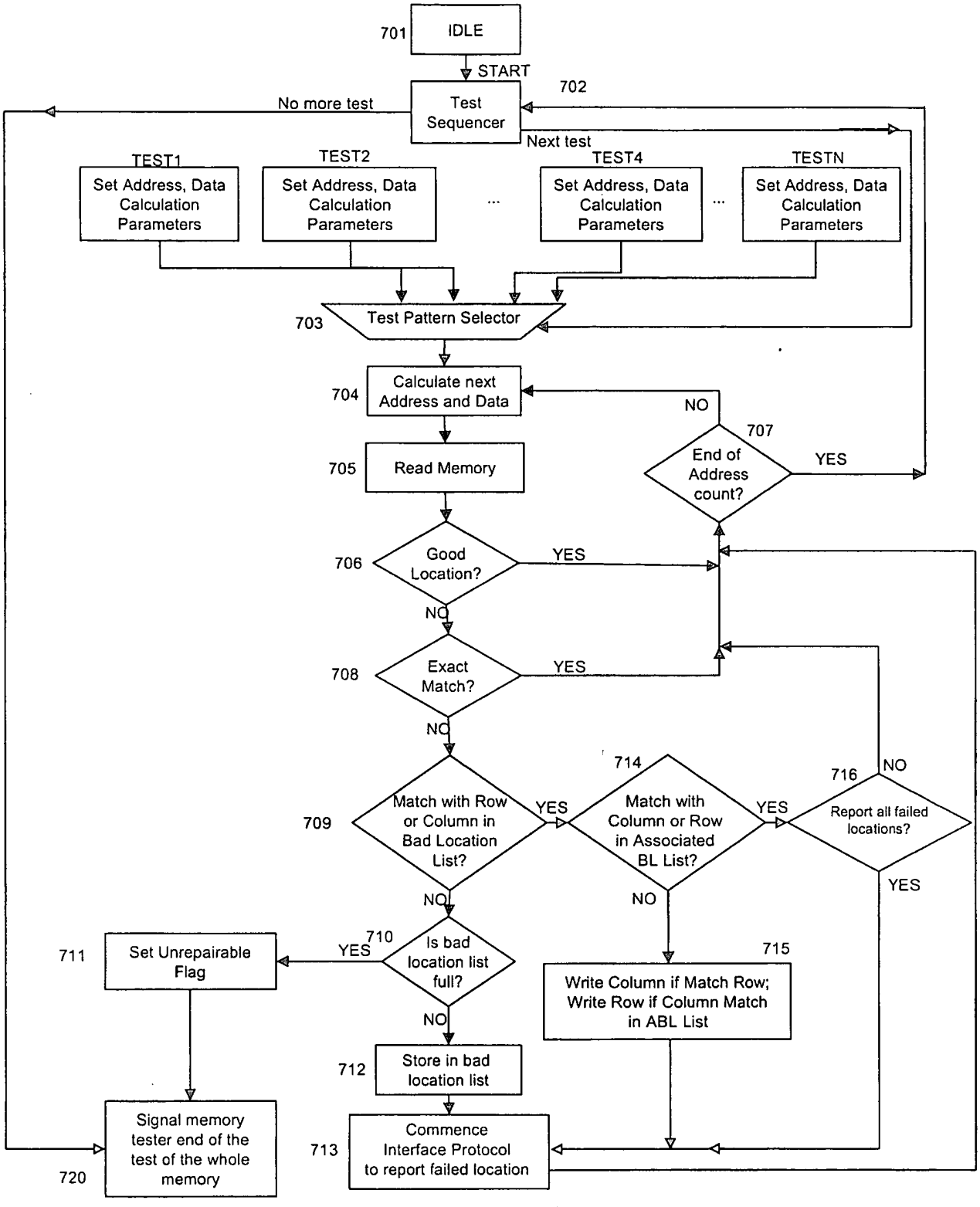
701
IDLE
START
702
Test Sequencer
No more test
Next test
TEST1
Set Address, Data Calculation Parameters
TEST2
Set Address, Data Calculation Parameters
TEST4
Set Address, Data Calculation Parameters
TESTN
Set Address, Data Calculation Parameters
703
Test Pattern Selector
704
Calculate next Address and Data
705
Read Memory
706
Good Location?
YES
NO
707
End of Address count?
NO
YES
708
Exact Match?
YES
NO
709
Match with Row or Column in Bad Location List?
YES
NO
714
Match with Column or Row in Associated BL List?
YES
NO
716
Report all failed locations?
NO
YES
710
Is bad location list full?
YES
NO
711
Set Unrepairable Flag
712
Store in bad location list
713
Commence Interface Protocol to report failed location
715
Write Column if Match Row; Write Row if Column Match in ABL List
720
Signal memory tester end of the test of the whole memory

FIG. 7

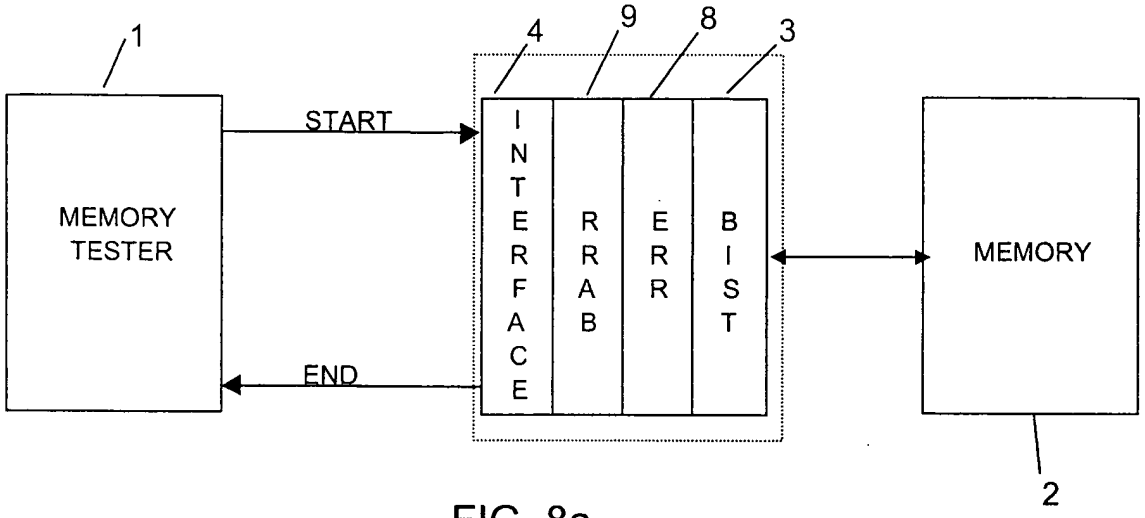
1
4
9
8
3
START
MEMORY TESTER
INTERFACE
RRAB
ERR
BIST
MEMORY
END
2

FIG. 8a

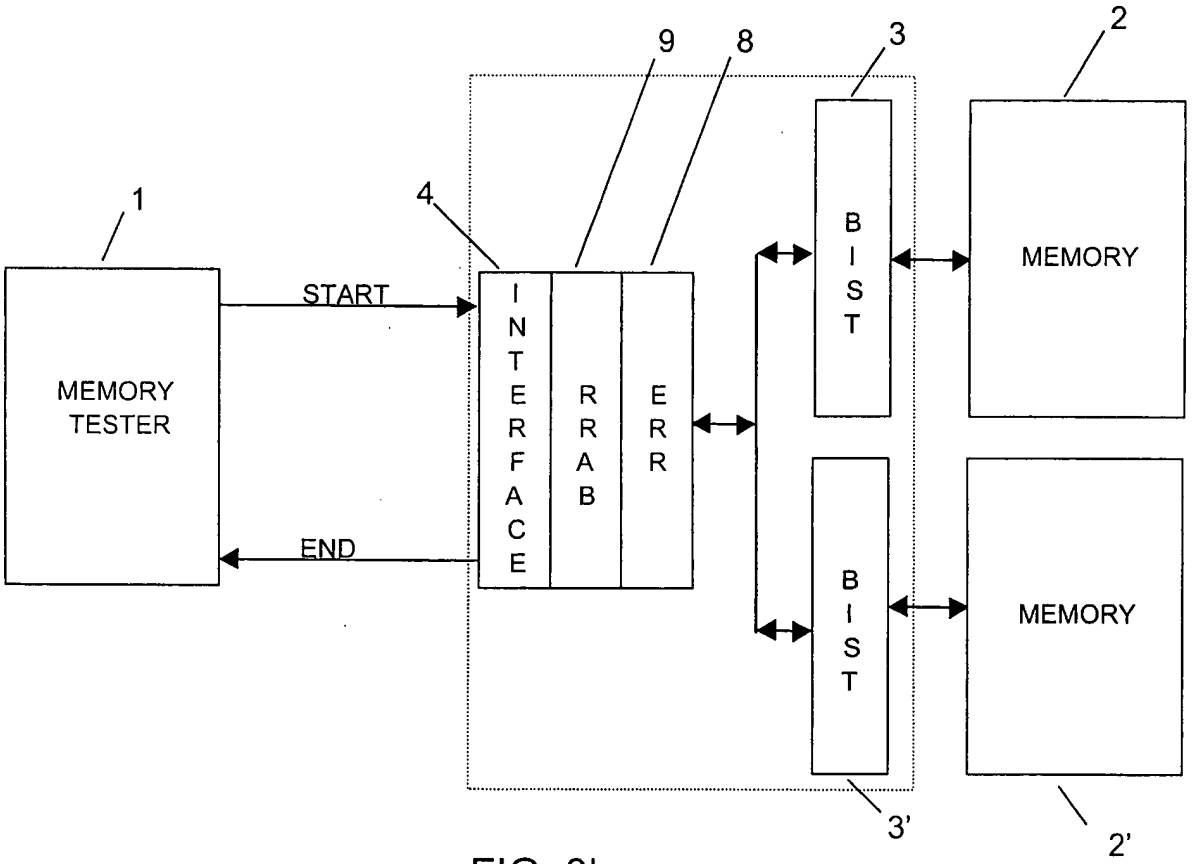
9
8
3
2
1
4
START
MEMORY TESTER
INTERFACE
RRAB
ERR
BIST
MEMORY
END
BIST
MEMORY
3'
2'

FIG. 8b

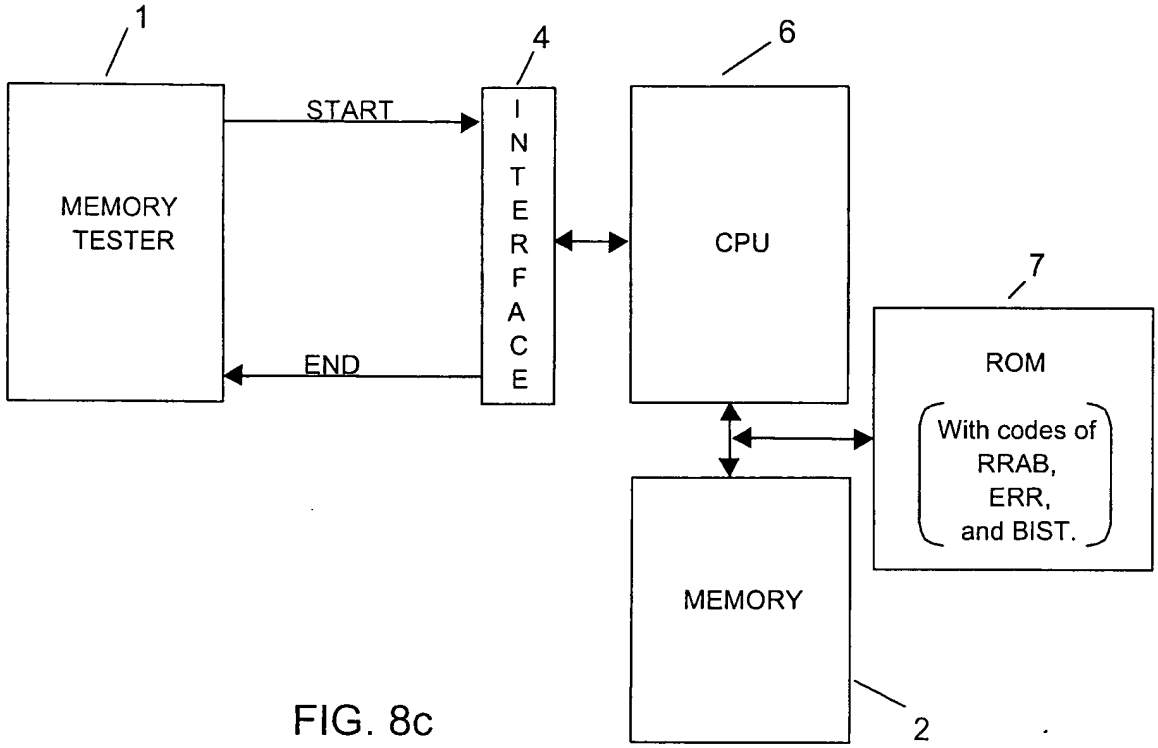
1
4
6
7
START
END
MEMORY TESTER
INTERFACE
CPU
ROM
With codes of RRAB, ERR, and BIST.
MEMORY
2

FIG. 8c

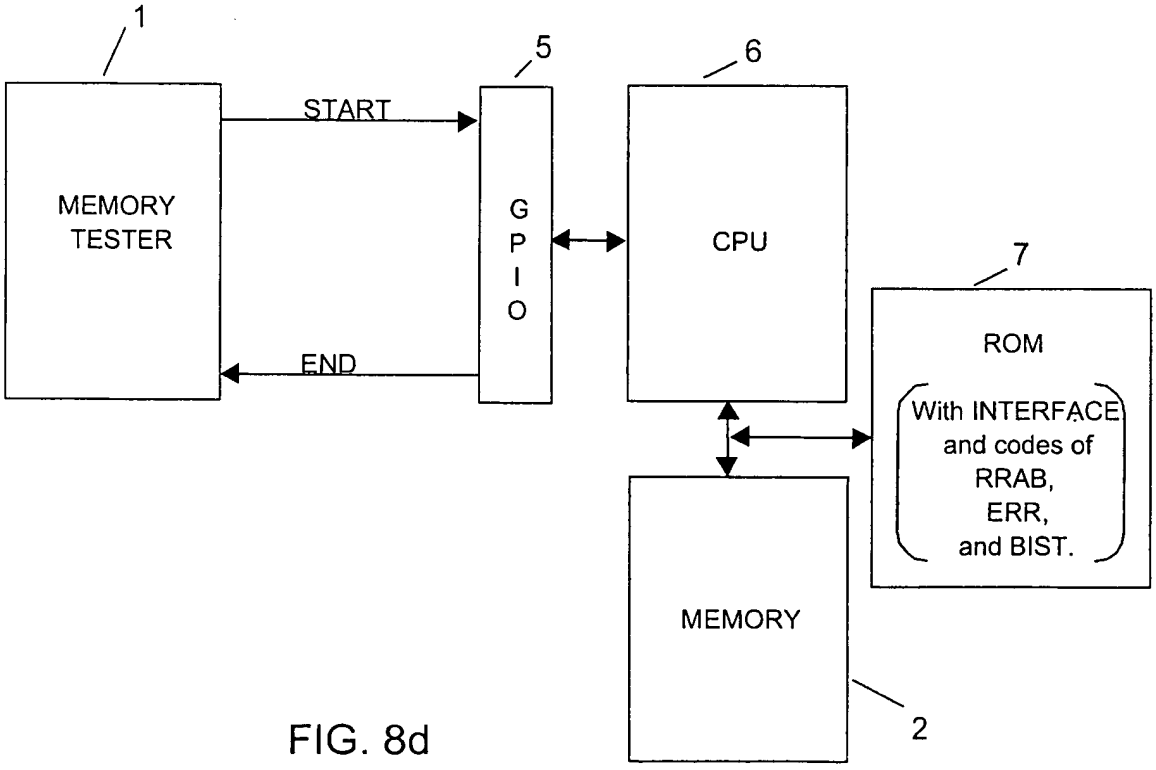
1
5
6
7
START
END
MEMORY TESTER
GPIO
CPU
ROM
With INTERFACE and codes of RRAB, ERR, and BIST.
MEMORY
2

FIG. 8d

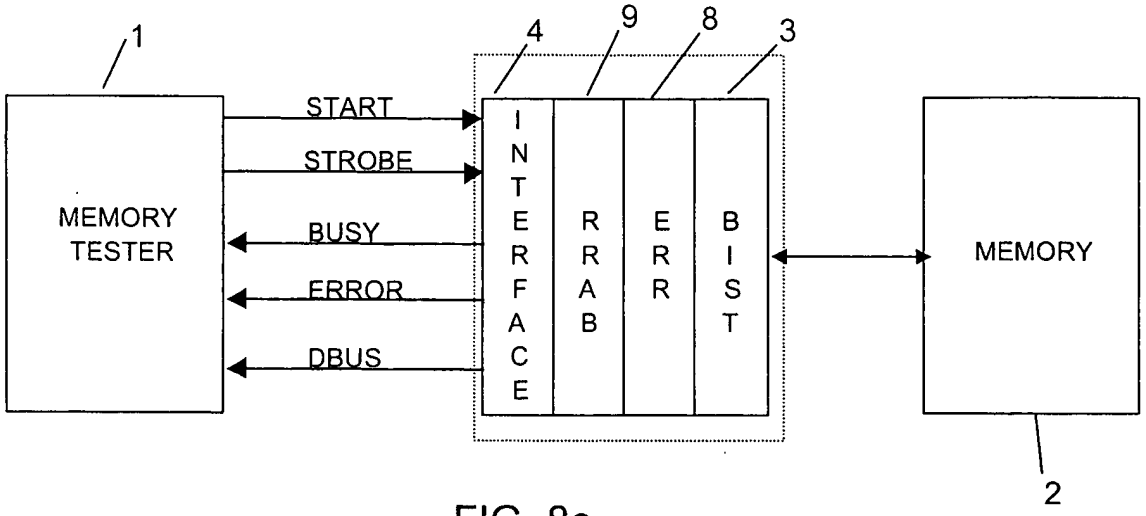
1
4
9
8
3
START
STROBE
BUSY
ERROR
DBUS
MEMORY TESTER
INTERFACE
RRAB
ERR
BIST
MEMORY
2

FIG. 8e

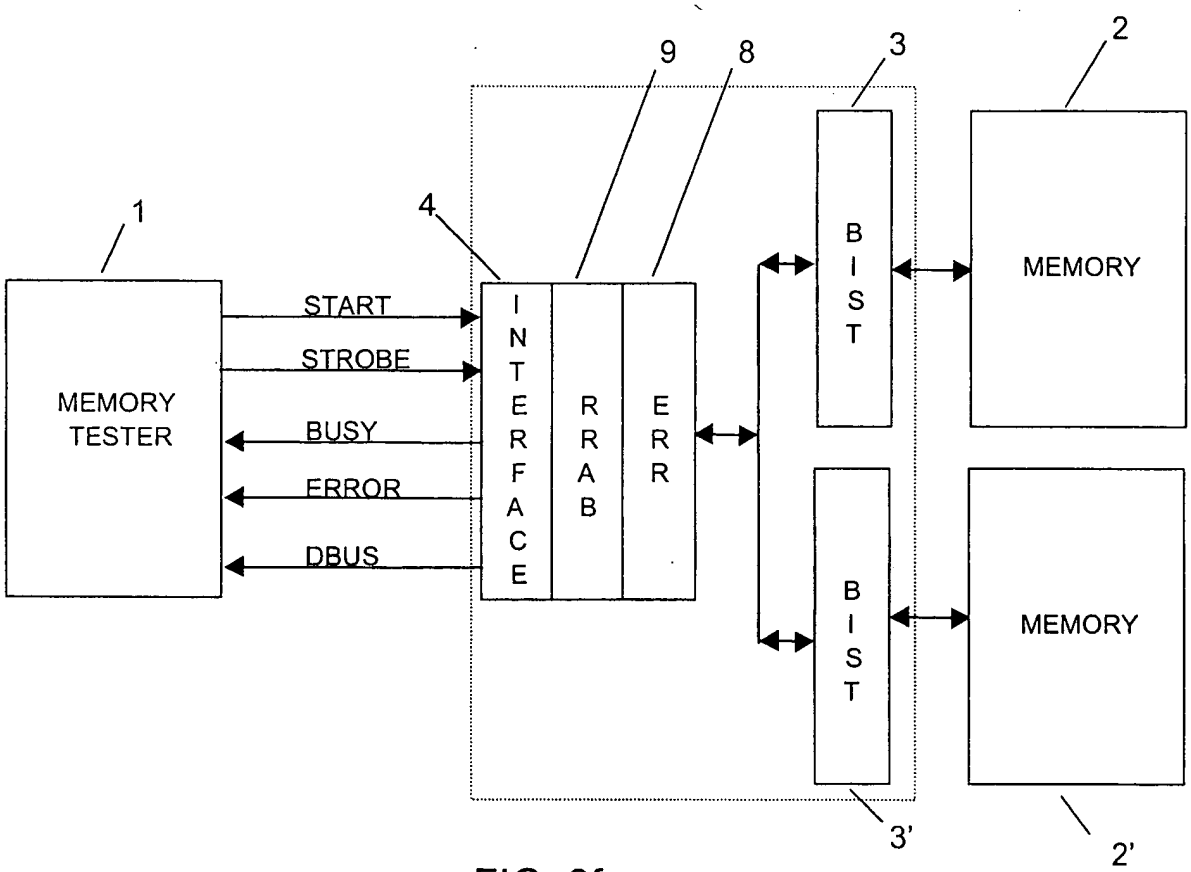
9
8
3
2
1
4
START
STROBE
BUSY
ERROR
DBUS
MEMORY TESTER
INTERFACE
RRAB
ERR
BIST
MEMORY
BIST
MEMORY
3'
2'

FIG. 8f

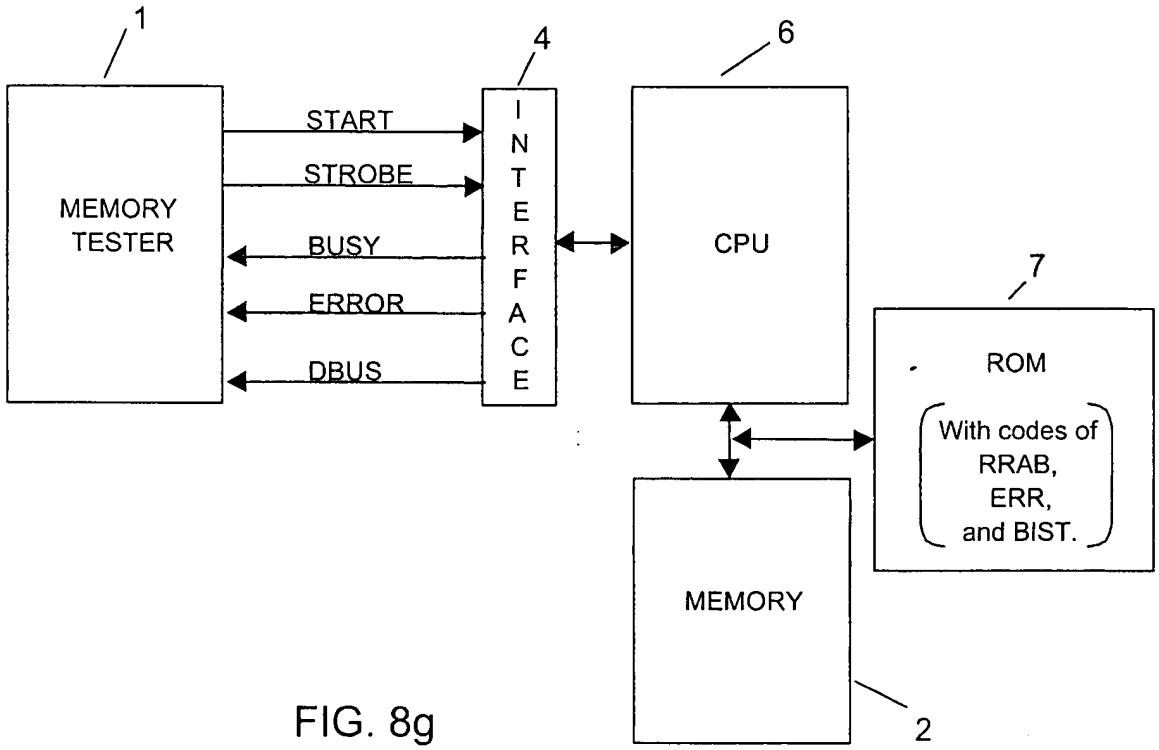
1
4
6
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
INTERFACE
CPU
7
ROM
With codes of RRAB, ERR, and BIST.
MEMORY
2

FIG. 8g

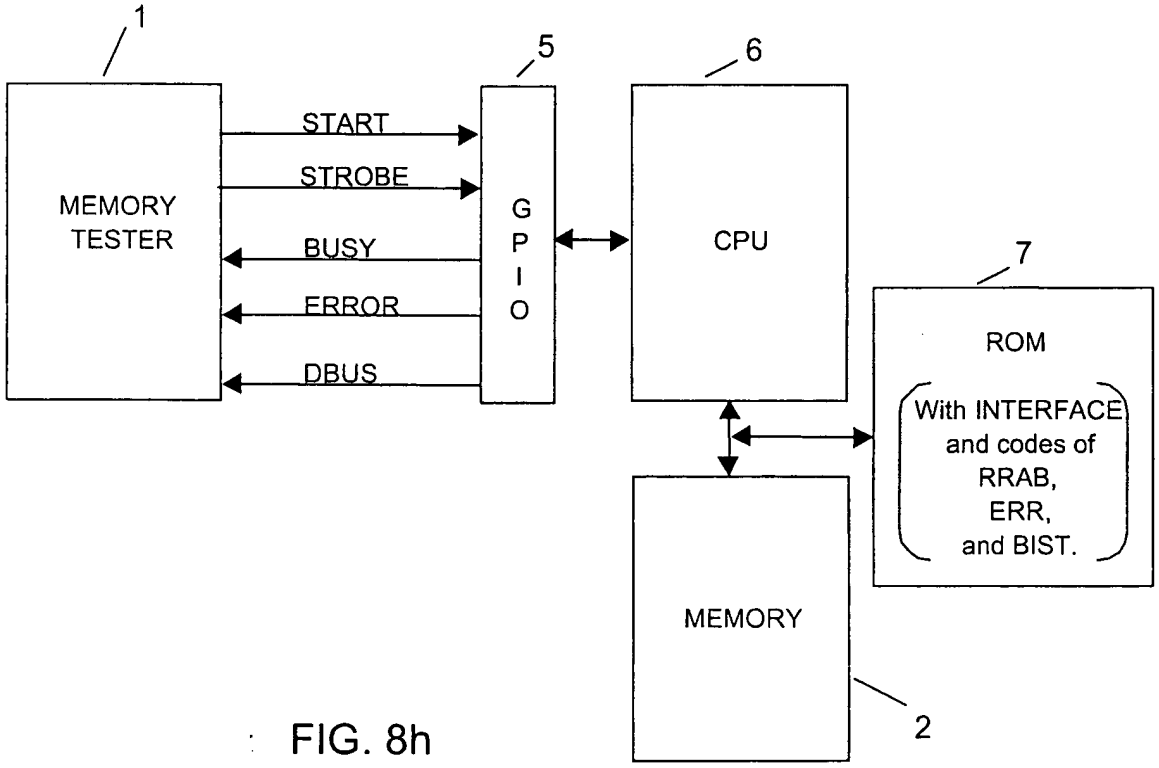
1
5
6
MEMORY TESTER
START
STROBE
BUSY
ERROR
DBUS
GPIO
CPU
7
ROM
With INTERFACE and codes of RRAB, ERR, and BIST.
MEMORY
2

FIG. 8h

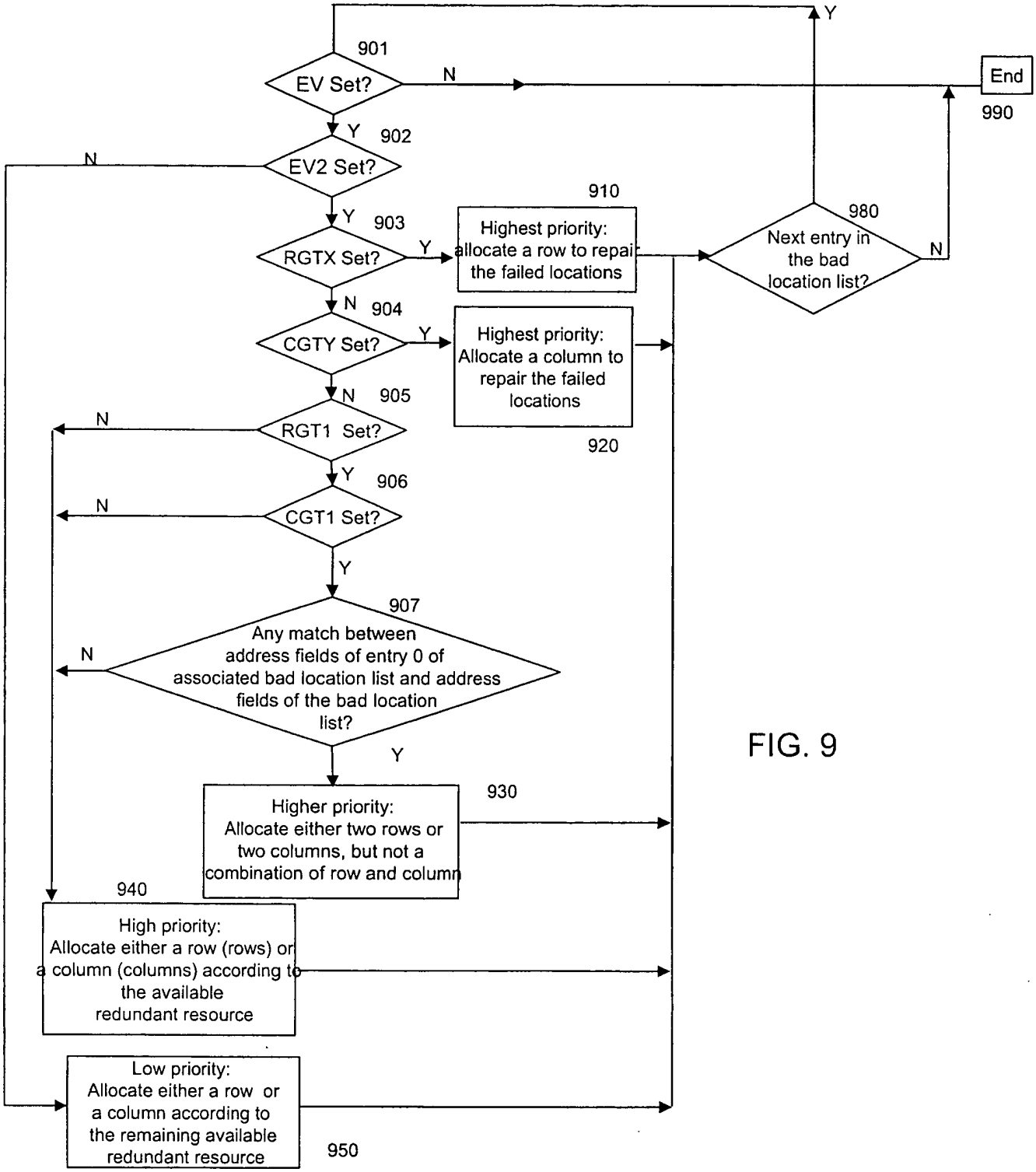
901
EV Set?
N
End
990
Y
902
EV2 Set?
N
910
Y
903
RGTX Set?
Y
Highest priority: allocate a row to repair the failed locations
980
Next entry in the bad location list?
N
Y
N
904
CGTY Set?
Y
Highest priority: Allocate a column to repair the failed locations
N
905
RGT1 Set?
N
920
Y
906
CGT1 Set?
N
Y
907
Any match between address fields of entry 0 of associated bad location list and address fields of the bad location list?
N
Y
930
Higher priority: Allocate either two rows or two columns, but not a combination of row and column
940
High priority: Allocate either a row (rows) or a column (columns) according to the available redundant resource
Low priority: Allocate either a row or a column according to the remaining available redundant resource
950

FIG. 9